

**IN THE CLAIMS:**

- 1    1. (Currently amended) A multiple-processor system comprising:
- 2            a)     A plurality of nodes, each node including one or more processors, a shared  
3    memory space, portions of which are resident in respective nodes;
- 4            b)     an inter-node switch unit linking each of the nodes with other nodes to  
5    provide the communication among the nodes, the switch unit serving as an ordering ordi-  
6    ~~nary~~ point for memory reference requests; said switch unit comprising:
- 7            1.     a plurality of input switches, each of which (a) is connected to receive  
8    messages transmitted by a different group of processors; (b) and is configured to transmit  
9    messages selectively over a plurality of inter-switch output terminals, and (c) issues  
10   atomic messages corresponding to each memory reference request from a node connected  
11   to that switch; and
- 12           2.     a plurality of output switches, each of which: (a) is connected to receive  
13   messages from an inter-switch output terminal of each of the input switches ~~and~~, (b) se-  
14   lectively transmits outputs to a group of nodes connected to that switch; and (c) follows  
15   the same ordering rule relative to input switches from which the messages are received  
16   simultaneously.
- 1    2. (Original) The system defined in claim 1 in which all of said input switches operate in  
2    synchronism with the same clock.
- 1    3. (Original) The system defined in claim 1 in which all of said output switches operate in  
2    synchronism with the same clock.

1 4. (Currently amended) The system defined in claim 1 in which

2 A. a source node containing a processor that issues a memory write request  
3 transmits the request to a home node of the memory location involved in the re-  
4 quest;

5 B. the home node transmits to the input switch connected thereto a message  
6 packet identifying (1) the memory location, (2), the processors having copies of  
7 contents of the memory location and (3) the processor that is the source of the re-  
8 quest; and

9 C. The input switch transmits (1) messages identifying the memory location to the  
10 processors identified in the message from the home node, and (2) acknowledge-  
11 ment message to the home node, the messages from the switch to the source node  
12 and the home node being transmitted no earlier than any of the other messages.

1 5. (New) The system defined in claim 2 in which all of said output switches operate  
2 in synchronism with the same clock.

1 6. (New) The system defined in claim 1 wherein:

2 the connections between the input switches and the output switches define paths,  
3 and

4 all paths maintain message order.

1 7. (New) The system defined in claim 1 wherein one or more of the atomic mes-  
2 sages corresponding to a memory reference request include a commit-signal structure in-  
3 dicating apparent completion of the memory reference request rather than actual comple-  
4 tion of the request.

- 1 8. (New) The system defined in claim 1 wherein the inter-node switch is configured
- 2 to impose a weak-ordering consistency mode wherein inter-reference ordering is imposed
- 3 by a memory barrier (MB) instruction inserted between sets of memory reference re-
- 4 quests.